Seongryong Oh
M.S. Student, CASYS Lab, KAIST (2024.02 ~ Present)
sroh@casys.kaist.ac.kr

Career Profile

Master's student at KAIST's CASYS Lab with a background in Electrical Engineering and Computer Science. Interest in system for AI, accelerator design using FPGA, accelerator and RISC-V integration.

Education

- B.S. in Electrical Engineering & Computer Science (Double Major), KAIST ,March 2018 – February 2024
- M.S. in AI Semiconductor, KAIST ,March 2024 – Present

Experience

- Undergraduate Student Research Intern, CASYS Lab (KAIST), June 2022 – November 2023

  • Contributed primarily to the hardware aspects and software simulation components for the "DaCapo [ISCA'24]" paper project.
  • Collaborated closely with Prof. JongSe Park on advanced research topics in system design and video analytics.

- Teaching Assistant

  • CS411 (Fall 2023): Assisted with project development on end-to-end Systolic arrays implemented on FPGA (PYNQ-Z2 board).
  • CS230 (Fall 2024): Supported course instruction and project facilitation.

- Co-Researcher, ACT Lab at UCSD 2024, November

  • Participated in a short-term research visit at the ACT Lab under Prof. Hadi Esmaeilzadeh.
  • Actively participate in research discussion and implement several accelerator simulators and compiler.
  • Research details are to be announced (TBA).

Projects

- RISC-V + Accelerator Integration.

  • Integrate the Cheshire RISC-V SoC from PULP group and Genesys from ACT LAB via Verilog programming.
  • Accelerator controlled by RISC-V, upon completion of its operation, generate interrupt so that RISC-V can handle interrupt. Check it using Questasim. .
  • Keywords: AXI, RISC-V, End-to-end, MMIO

- RISC-V + NPU (Systolic Array) for MLP Task (MNIST), KAIST, Spring 2024

• Integrated an NPU (systolic array) with a RISC-V processor via the APB communication protocol.
• Verified the functionality of an MLP model (using the MNIST dataset).
• Keywords: MMIO, ARM AHB-Lite, NPU, Systolic array.
• Note: This project is in the verification stage and has not been synthesized yet.

- Building End-to-End FPGA Systolic Array, KAIST, July 2023 – September 2023

• Developed and implemented a systolic array on a PYNQ-Z2 FPGA board.
• Demonstrated the board running a real image detection model as part of a major course project (KAIST CS411).
• Keywords: FPGA, End-to-end accelerator, Verilog, VIVADO.

Publication

• DaCapo: Accelerating Continuous Learning in Autonomous Systems for Video Analytics

- Co-authored with Yoonsung Kim, Changhun Oh, Jinwoo Hwang, Wonung Kim, Seongryong Oh, Yubin Lee, Hardik Sharma, Amir Yazdanbakhsh, and Jongse Park.
- Presented at ISCA 2024 (Distinguished Artifact Evaluation Award).

Skills & Proficiency

• Programming Languages: Python, C, CUDA
• Hardware Design : RTL design using Verilog, Chisel, SystemVerilog
• Hardware Design Tools: Questasim, Vivado, Design Compiler, VCS